Exhibit A

REMARKS

I. Introduction

On May 31, 2016, the Patent Trial and Appeal Board (the "Board") issued a Decision affirming the Examiner in part. In the Decision, the Board issued a number of new grounds of rejection. (Decision at 102.) The Patent Owner responds by respectfully requesting to reopen prosecution before the Examiner pursuant to 37 C.F.R. § 41.77(b)(1). This Response includes both claim amendments and evidence – the accompanying Second Supplemental Declaration of Dr. Carl Sechen pursuant to 37 C.F.R. § 1.132 – to overcome the new grounds of rejection.

With respect to the claim amendments, the Patent Owner has made the following principle amendments to overcome the new grounds of rejection:

- Phase Lock Loop (PLL) Device
- Register
- Logic Element

The amendments are detailed in Section II. The Patent Owner respectfully submits that the claims, as amended, overcome the new grounds of rejection as detailed in Sections III-VI and in the accompanying Second Supplemental Sechen Declaration.

II. Claim Amendments and Discussion of Support

The '912 Patent has four original independent claims: claims 1, 15, 28, and 39. Previously, claims 52, 57, 67, 77, 82, and 87 were added independent claims. The amendments to the claims are discussed below with a discussion of support pursuant to 37 C.F.R. §§ 1.530(e) and 1.941. It is also noted that Section I of the Second Supplemental Sechen Declaration ("Second Supp. Sechen Decl.") provides a detailed analysis of the support for the claim amendments.

A. Phase Lock Loop (PLL) Device

Claim 1 is amended to recite (exemplary support citations in curly braces):

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, in response to signals received from the computer system {5:28}, the phase-lock loop (PLL) device {50 in Figs. 1A, 1B} transmits a PLL clock signal {5:29} to the plurality of DDR memory devices, the logic element, and the register {5:29-31}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Supp. Sechen Decl. at ¶ 10.

B. Register

Next, the Patent Owner has amended claim 1 to recite (exemplary support citations in curly braces):

> a register…
>
> wherein, the register {60 in Figs. 1A, 1B} (i) receives, from the computer system {5:31}, and (ii) buffers, in response to the PLL clock signal {Figs. 1A, 1B; 5:31}, a plurality of row/column address signals {7:43-45} and the bank address signals {7:50-51}, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices {30 in Figs. 1A, 1B; 5:34-36}, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register {A_0-A_n in Figs. 1A, 1B} are separate from the at least one row address signal received by the logic element {A_{n+1} in Figs. 1A, 1B}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 11.

C. Logic Element

Additionally, claim 1 is amended to recite (exemplary support citations in curly braces):

> the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, …
>
> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals {Figs. 1A, 1B, 3A, 3B; 17:28-19:52l 22:50-63; 23:6-25} of the output control signals in response {6:55-63} at least in part to (i) the at least one row address signal {A_{n+1} in Figs. 1A, 1B; A13 in Figs. 3A, 3B; 7:46-53}, (ii) [a] the bank address signals {B_0-B_m in Figs. 1A, 1B; BA_0, BA_1 in Figs. 3A, 3B; 7:46-53}, and (iii) the at least one chip-select signal {CS_0, CS_1 in Fig. 1A; CS_0 in Fig. 1B; 7:46-53} of the set of input control signals and (iv) the PLL clock signal {Figs. 1A, 1B; 5:29-30; "clk_in" in 17:28-19:52}.

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 12.

D. Other Amendments

A number of other amendments were made for conformity.

The dependency of claim 43 has been changed to claim 39 in view of the cancellation of claim 42.

The dependency of new claim 54 has been changed to new claim 52 in view of the cancellation of new claim 53. The recitation of "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" previously in new claim 54 has been deleted in view of the amendment to new claim 52.

In new claim 123, the recitation "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating" has been replaced by "the chip-select signals generated by the logic element are" in view of the amendment to claim 1.

The dependency of new claim 125 has been changed to new claim 123 in view of the cancellation of new claim 124. The phrase "the row address bit" has been changed to "the at least one row address signal" and the recitation "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" has been deleted in view of the amendment to claim 1.

The dependency of new claim 131 has been changed to claim 1 in view of the cancellation of new claims 128-130.

The dependency of new claim 134 has been changed to claim 15 in view of the cancellation of claim 25.

The term "the bank address signals" has been deleted from claims 134-136 in view of the amendments to claims 15, 28 and 39.

III. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122, and 132-136 Are Patentable Over Amidi In View Of Dell 2 (Ground 5)

Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29 , 31, 32, 34-43, 45-50, 120-122 and 132-136 have been rejected by the Board as obvious over Amidi in view of Dell 2. These amendments distinguish the claims from the combination of Amidi and Dell 2. *See* Second Supp. Sechen Decl. at Section II.

Dell 2 is cited for teaching or suggesting "a logic element receiving and using free signals, including a bank address signal", and Amidi is cited for its "suggestion to use other types of

memory devices." (Decision, 43.) The Decision then concludes that the combination of Amidi and Dell 2 teaches or suggests generating a chip-select, CAS, or rank selecting signal in response to a bank address signal. (Decision, 81.) To address the Board's rejection, Patent Owner narrowed the claim to include:

- "in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register"
- "the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element"
- "the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal."

As described herein, the claim amendments highlight at least two differences between the '912 invention and the prior art.

First, the claim amendments now require: in response to signals received from the computer system, the phase-lock loop (PLL) device transmit a PLL clock to the plurality of DDR memory devices, the logic element, and the register. Amidi transmits a PLL clock signal to the register and memory, but not to the CPLD. Thus, Amidi does not disclose the PLL device transmitting the PLL clock to the *logic element*; the output of PLL 606 is neither directly nor indirectly transmitted to the

CPLD 604. *See* Second Supp. Sechen Decl. at ¶¶ 18-19. Additionally, a POSITA would not be motivated or inclined to transmit the PLL clock to CPLD 604. *Id.* at ¶ 20.

Second, the amended claims now also require that the logic element generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals. Instead, the control signals (rcs0a, rcs0b, rcs1a, rcs1b, rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select signals. Thus, Amidi does not disclose the CPLD generating the gated CAS signals or chip-select signals in response to *the bank address signals*. Second Supp. Sechen Decl. at ¶¶ 21-22. Moreover, since the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604, a POSITA would understand that the PLL clock does not control the operation of CPLD 604. Thus, Amidi is further deficient by failing to disclose the CPLD generating the gated CAS signals or chip-select signals in response to the *PLL clock signal*. *Id.* at ¶ 18-19.

Dell 2 does not cure the deficiencies of Amidi with respect to the amended claim. Dell 2 merely discloses a remapping or reassignment of a row address bit (A12) to be used as a bank address bit (BA1). Dell 2 does not disclose using bank address signals to generate a chip-select signal or a CAS signal. Second Supp. Sechen Decl. at ¶ 25.

Even taken in combination, Amidi and Dell 2, it would not be obvious to a POSITA to modify Amidi's system to provide the bank address signals to the CPLD device, and generate chip-select signals based on the bank address signals and a row address signal. As amended, the claims require that the *logic element receives* at least one row address signal and *bank address signals*, and require that *the register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices. The claims also require the plurality of row/column

address signals received by the register are separate from the at least one row address signal received by the logic element. In other words, in the configuration recited by the claims, the bank address signals are received by the logic element, the register and the plurality of memory devices. Under such circumstances, Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and the at least one row address signal). The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals. Second Supp. Sechen Decl. at ¶¶ 23-24 and 26.

Based on the above, it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

While claims 132-133 are patentable over Ground 5 based on amended claim 15 from which they depend, these claims are patentable for an additional reason. Specifically, claim 132 (and its dependent claim 133) recite that "the command signal is transmitted to only one DDR memory device at a time." Claim 16 (and its dependent claim 17) have a similar recitation, and the Board found that Amidi and Dell 2 were deficient as to this recitation. (Decision, 75-77, 82-83.) Based on that reasoning, claims 132 and 133 are similarly patentable over Ground 5. It is believed that the inclusion of these claims under Ground 5 has been in error.

IV. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 Are Patentable Over Micron In View Of Amidi (Ground 13)

Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 have been rejected by the Board as obvious over Micron in view of Amidi.

The Decision relied on two different cases proposed by Requester 3 to reject the claims. The first case refers to a memory controller that generates one row address signal more than the actual